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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Paper No. 18

Application Number: 09/186,584

Filing Date: November 5, 1998

Appellant(s): Greenfield et al

Kevin P. Radigan

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 15, 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellants' brief includes a statement that the claims are grouped into the following two groups: Group I, claims 1-6, 16-19, 32, and 34; and Group II, claims 7-15, 20-31, 33, and 35. At page 6 of the brief filed January 15, 2003, the appellants however provide a statement that the claims of Group I do not stand and fall together and the claims of Group II do not stand or fall together. Such statement is contradictory since the appellants have argued in the argument section of the brief filed January 15, 2003 (see pages 7-12 of the brief) why the claims of the Group I are separately patentable from the claims of Group II, and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8). The correct grouping of the claims should therefore be as follows: the claims of Group I stand or fall together and the claims of Group II stand or fall together.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,760,836	GREENFIELD et al	6-1998
6,094,696	CHOE et al	6-2000

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

1. Claims 1-6, 16-19, 32, and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Greenfield et al of record (5,760,836).

Greenfield et al discloses a FIFO feedback and control for digital video encoder as shown in Figures 1 and 5, and the same method and encoder as claimed in claims 1-6, 16-19, 32, and 34 for encoding a digital video image stream in the encoder (see Figure 1), comprising means (21 of Figure 1) for spatial compression of still images in the digital video image stream and means (41 of Figure 1) for temporal compression between the still images, wherein the means for spatial compression comprises means for converting a time domain image of a macroblock to a frequency domain image of the macroblock (see column 1, lines 55-63), means for taking a discrete cosine transform of the frequency domain image (see column 1, lines 55-63), means for transforming the discrete cosine transformed macroblock image by a quantization factor (see 23 of Figure 1), and means for run length encoding the quantized discrete cosine transformed macroblock image (see 25 of Figure 1), wherein the means for temporal compression comprises means for reconstructing the quantized, discrete cosine transformed image of the macroblock (see Figure 1), means for searching for a best match macroblock, and means for constructing a motion vector therebetween (see column 6, line 55 to column 7, line 11), the encoder for encoding thereby forming a bitstream comprising run length encoded,

quantized, discrete cosine transformed macroblocks and motion vectors and passing the bitstream to and through an external buffer to a transmission medium (see column 6, line 55 to column 7, line 11), comprising means for feeding back to hardware logic (i.e., as provided by the buffer management system of Figure 5) within the encoder an external read signal from a host (see 51 and FIFO_RD of Figure 5, and columns 5-7), and for incrementing an on-chip counter of the hardware logic each time that the external buffer is read and calculating therefrom the number of bits read by a host (see column 5, lines 31-50), the hardware logic in the encoder being further adapted to monitor a number of bits encoded and written into the external buffer and subtract from the number of bits encoded the number of bits read by the host to continuously obtain the fullness of an external buffer, wherein the continuously obtaining comprises obtaining the fullness of the external buffer every cycle of the encoder (i.e., by having a real time encoding system, real time fullness of the external buffer is maintained every cycle of the encoder, see column 1, lines 32-49, column 5, lines 24-30, lines 53-59), and wherein the hardware logic in the encoder is further adapted to provide the host with a dynamic buffer level indicator in real time indicative of the fullness of the external buffer (i.e., the external buffer BF is being monitored until the bitrate is adjusted to meet the criteria BF<L, with the amount of time the bitrate being adjusted changed as desired using microcode, thereby providing a dynamic buffer level indicator, see column 5, lines 24-67, columns 6-7); wherein the logic adapted to provide the host with a dynamic buffer level indicator comprises logic adapted to continuously compare the real time fullness of the external buffer (i.e., by having a real time encoding system, real time fullness of the external buffer is maintained, see column 1, lines 32-49, column 5, lines 24-30, lines 53-59), with a buffer threshold defined by the host and to provide a high level indicator when the buffer fullness is greater than the buffer threshold and a low level indicator when the buffer threshold is greater than the buffer fullness (see column 6, lines 18-29);

further comprising a buffer threshold register (153 of Figure 5) within the encoder coupled to the logic adapted to compare the buffer fullness to the buffer threshold, wherein the external buffer comprises at least one FIFO buffer (see column 1, column 6, lines 18-45, and Figure 5); an external buffer configuration register (151 of Figure 5) in the encoder for retaining multiple external buffer configuration values, and wherein the calculating in the encoder the number of bits read by the host includes employing a predefined configuration value of the external buffer configuration register in determining the number of bits read by the host upon receipt of each buffer read signal from the host, and wherein the multiple external buffer configuration values retained in the external buffer configuration register comprise at least some of 1, 2, 4, and 8 byte buffer configuration values, each value being representative of a number of bytes read from the external buffer with each buffer read signal from the host for a respective external buffer configuration (see column 5, lines 31-50).

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 7-15, 20-31, 33, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greenfield et al as applied to claims 1-6, 16-19, 32, and 34 in the above paragraph (1), and further in view of Choe et al of record (6,094,696).

Greenfield et al discloses substantially the same method and encoder for encoding a digital video image stream in the encoder as above, further including wherein the external buffer comprises one of a field buffer or cascaded FIFO buffers (see Figure 5), continuously comparing the fullness of the external buffer to

a predefined buffer size and providing the host with a high level indicator when the buffer fullness is greater than or equal to the buffer size and a low level indicator when the buffer size is greater the buffer fullness, and providing an on chip buffer size register for holding a host defined buffer size value for use in the comparing of the buffer fullness to the buffer size (see columns 5-6).

Greenfield et al does not particularly disclose, though, providing from the encoder to the host in real time a dynamically updated flag comprising at least one of a buffer empty flag, a buffer almost full flag and a buffer full flag as claimed in claims 7-11, 13, 20-22, 24, 27, and 29-31. However, Choe et al discloses a virtual serial data transfer mechanism and teaches the conventional use of a buffer management system wherein buffer full and buffer empty flags are set (see column 2, line 62 to column 3, line 56). Therefore, it would have been obvious to one of ordinary skill in the art, having the Greenfield et al and Choe et al references in front of him/her and the general knowledge of flag indicating statuses for a buffer management system, would have had no difficulty in providing the dynamic buffer flagging system as taught by Choe et al as part of the buffer management within Figure 5 of Greenfield et al for the same well known flag identification purposes as claimed.

(11) Response to Argument

Regarding the appellants' arguments at pages 7-9 of the brief filed January 15, 2003 concerning in general that "... Agnes Y. Ngai, co-inventor of the present invention and co-inventor on the Greenfield patent, has provided a characterization of the teachings and capabilities of the Greenfield system which supports the differences discussed below with respect to the system ... Greenfield et al fails to uncover any teaching, suggestion or implication that the processing or logic described therein comprises a dynamic buffer level indicator that is provided as recited by appellants herein. In fact, Greenfield et al specifically describes a

non-real time buffer level indicator. In Greenfield, the buffer level indicator is provided dependent upon how often the processor updates the indicator. The hardware described in Greenfield would be incapable of supporting a continuously obtaining application as recited herein ... In other words, while the processor is doing the updating of the buffer level indicator, the buffer level signal is not returned on a continuous basis. As one example, in the Greenfield system, a buffer level indicator would be returned approximately once per picture frame ... In contrast, appellants' hardware logic continuously obtains the fullness of the external buffer ... it is implemented in microcode, and therefor, buffer fullness is not constantly monitored ...", the Examiner wants to point out that the Agnes Y Ngai Declaration filed November 25, 2002 and arguments presented above in connection with the Ngai Declaration have been considered, but such arguments and Ngai Declaration are deemed not persuasive for the following reasons. It is again that though Greenfield et al uses a microcode operation for detecting overflow, Greenfield et al is nevertheless also interested in continuously obtaining the fullness of the external buffer BF. Greenfield teaches that the external buffer BF needs to be monitored to thereby provide an adjusted bitrate satisfying the criteria BF<L in order to prevent buffer overflow (see column 5, lines 24-67). In order to meet the criteria BF<L, the fullness of the external buffer BF would inherently have to be continuously monitored. Otherwise, buffer overflow results. Therefore, it is submitted again that Greenfield et al (see column 5, lines 24-30, lines 53-67) shows the same hardware logic in the encoder being adapted to monitor a number of bits encoded and written into the external buffer and subtract from the number of bits encoded the number of bits read by the host to continuously obtain the fullness of an external buffer as claimed.

Regarding the appellants' arguments at pages 9-11 of the brief filed January 15, 2003 concerning in general that "... appellants continuously attain the recited dynamic buffer level indicator through the use of a

hardware implementation. As noted above, Greenfield describes a microcode implementation, which, based on the processing described therein, comprises a non-continuous implementation. This is understood by one skilled in the art through the use of a non-real time counter to monitor the amount of data written to the FIFOs in Greenfield et al (see column 6, lines 10-11), and through the use of a non-continuous sampling of this counter by the microcode ... However, these columns teach, suggest or imply continuous monitoring of external buffer fullness, as recited in appellants' independent claims. As discussed in the Ngai Declaration at page 2, lines 17-24, Greenfield's real time encoding system means that the encoder therein is capable of completing calculations necessary to encode pictures at a rate specified by a relevant standard ... Thus, the "real time" aspect of Greenfield's system is different from and independent of appellants' recited continuous monitoring of external buffer fullness ... The Ngai Declaration clearly establishes that the Greenfield system does not provide any means to continuously obtain the fullness of the external buffer, and one skilled in the relevant art would not expect Greenfield's hardware logic to be capable of being modified to continuously obtain buffer fullness ... This continuous obtaining of the external buffer fullness every encoder cycle is quite different from Greenfield's buffer indicator ...", the Examiner respectfully disagrees. It is again that continuous monitoring/obtaining of the fullness of the external buffer BF is required in order to prevent buffer overflow and satisfy the criteria BF<L within Greenfield et al, and with the continuous obtaining of the fullness of the external buffer being determined every cycle of the encoder (see column 5, lines 24-30, lines 53-67, columns 6-7). And it is submitted again that since real time encoding is realized within Greenfield (see column 5, lines 24-30), and the processings and monitorings of the external buffers are provided in real time as taught by Greenfield, appellants' arguments that the microcode implementation of Greenfield comprises a non-real time counter to monitor the amount of data written to the FIFOs are not

convincing. For the encoding system of Greenfield et al to be provided in real time as described at column 5, lines 24-30, all components/processings within the encoder must inherently be performed in real time as well.

Regarding the appellants' arguments at pages 11-13 of the brief filed January 15, 2003 concerning in general that "... Each independent claim at issue (i.e., claims 9 & 27) recites a technique wherein hardware logic within the encoder continuously obtains and provides to the host a dynamically updated flag. Neither Greenfield et al nor Choe et al continuously obtain and provide from encoder hardware to a host a dynamically updated flag ... Greenfield et al fails to uncover any teaching, suggestion or implication of hardware logic implementing a technique wherein a dynamic buffer level indicator is continuously obtained and provided to a host. Similarly, a careful reading of Choe et al fails to uncover any discussion of an encode process, let alone the provision of a dynamic buffer level indicator from an encoder to a host ... This is in contrast with the flags disclosed by appellants which are dynamic, real time indicators ... The flags of Choe et al are used to start data transfer operations ... Appellants' flags are used to regulate data rate in and out of the FIFOS in a simultaneous and continuous manner ... In appellants' recited invention, hardware logic within the encoder performs certain functions, including subtracting from a number of bits encoded the numbers of bits read by the host to continuously obtain the fullness of an external buffer ... the applied art fails to uncover any suggestion or capability that the systems described therein could obtain the fullness of the external buffer every cycle of the encoder ...", the Examiner wants to point out that since the external buffer BF of Greenfield et al is being continuously monitored until the bitrate is adjusted to meet the criteria BF<L, with the amount of time the bitrate being adjusted changed as desired using microcode (see column 5, line 24 to column 6, line 17 of Greenfield), it is submitted again that the hardware logic in the encoder of Greenfield thereby provides to the host with a dynamic buffer level indicator in real time indicative of the fullness of the

external buffer as claimed. In addition, the hardware logic within the encoder of Greenfield et al provides the same subtracting from a number of bits encoded the numbers of bits read by the host (i.e., equation BF, see column 5, line 59) to continuously obtain the fullness of an external buffer every cycle of the encoder (see column 5, lines 24-30, lines 53-67). And since Choe et al teaches the conventional buffer management system with buffer full and buffer empty flags being able to be set (see column 2, line 62 to column 3, line 56), it is submitted that it is considered obvious to provide the buffer flagging system of Choe et al for the buffer management system of Greenfield et al to thereby provide substantially the same if not the same encodings within Greenfield in real time with a dynamically updated flag comprising at least one of a buffer empty flag, a buffer almost full flag and a buffer full flag as claimed. For reasons above, it is further submitted that the claimed invention is rendered obvious in view of the combination of Greenfield et al and Choe et al.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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